

Notice of References Cited	Application/Control No. 10/041,671	Applicant(s)/Patent Under Reexamination ADIR, ALLON	
	Examiner SHAMBHAVI PATEL	Art Unit 2128	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-			
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
*	U	Genie: Genesys-MP User's Guide. Chapters 1-4, 1999.
*	V	Luo et al. "Development and Validation of a Hierarchical Memory Model Incorporating CPU- and Memory- Operation Overlap", ACM 1998.
	W	Saha et al. "A Simulation Based Approach to Architectural Verification of Multiprocessor Systems", IEEE 1995.
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.